SWIFT-SAT: Unlimited Radio Interferometry: A Hardware-Algorithm Co-Design Approach to RAS-Satellite Coexistence

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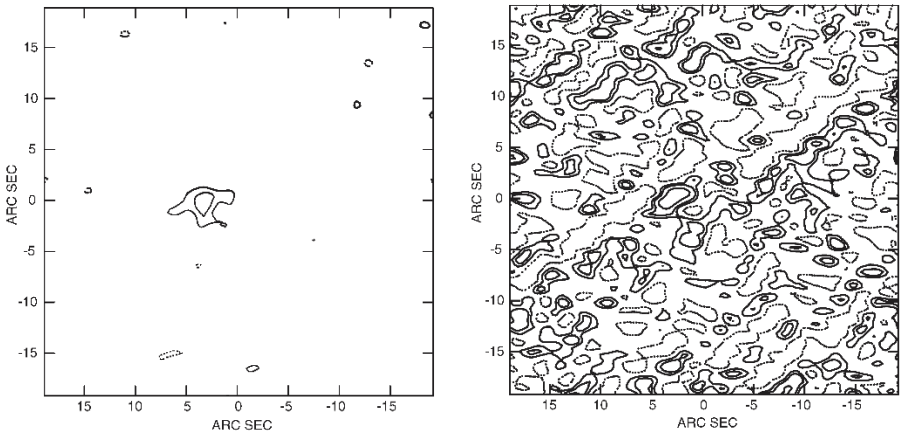
Project Objective

- Satellite RFI Threatens Radio Astronomy
  - ADC Saturation Risk
    - ✓ Mega-constellations greatly increase main-beam RFI exposure
    - ✓ High-power signals can saturate telescope receivers
  - Conventional RFI cancellation fails under saturation



Left: VLA image of a star. Right: Same star when a satellite was passing by [1].

- Objective: Enhance RAS receiver linearity to tolerate high input power via a hardware-algorithm co-design for RAS-satellite coexistence
- Technical Innovations
  - Modulo Sampling Framework:
    - ✓ recovers HDR (high dynamic range) information from LDR measurements
    - ✓ enables unlimited radio interferometry
  - Robust and super-resolution interferometric imaging
  - Scalable modulo ADC design for unlimited interferometry capability in strong RFI

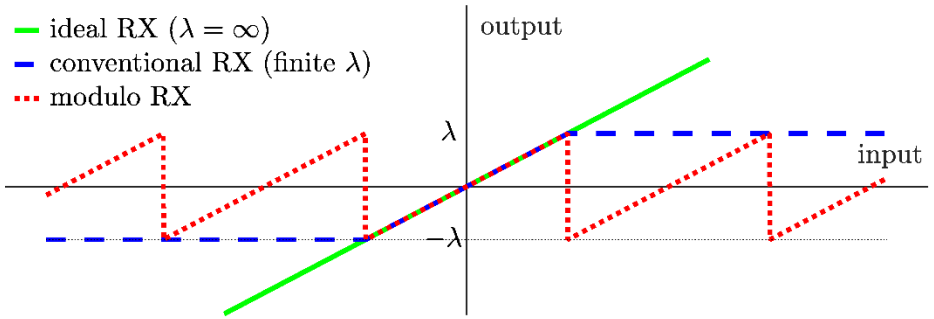
[1] National Research Council, *Spectrum Management for Science in the 21st Century*. National Academies Press, 2010.

Modulo Sampling and Reconstruction

- Modulo sampling:

$$y = \mathcal{M}_\lambda(x) = 2\lambda \left\langle \frac{x+\lambda}{2\lambda} \right\rangle - \lambda$$

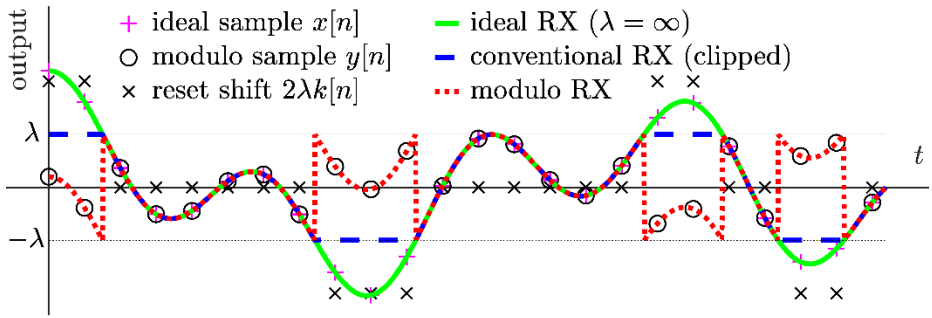
$$\langle x \rangle = x - \lfloor x \rfloor$$



Transfer functions of 3 types of receivers (RXs)

- Reconstruction by high-order finite differences:
  - HDR samples $x[n]$ can be efficiently recovered from LDR modulo measurements $y[n]$ by leveraging the fact (for sufficiently large J)

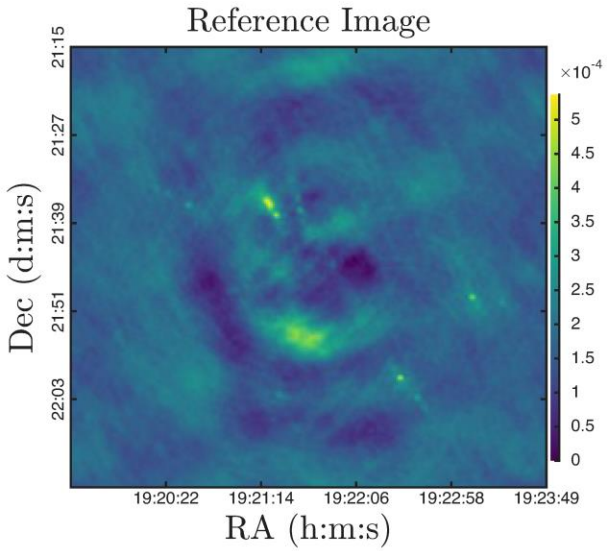
$$\Delta^J(x[n]) = \mathcal{M}_\lambda\left(\Delta^J(y[n])\right)$$



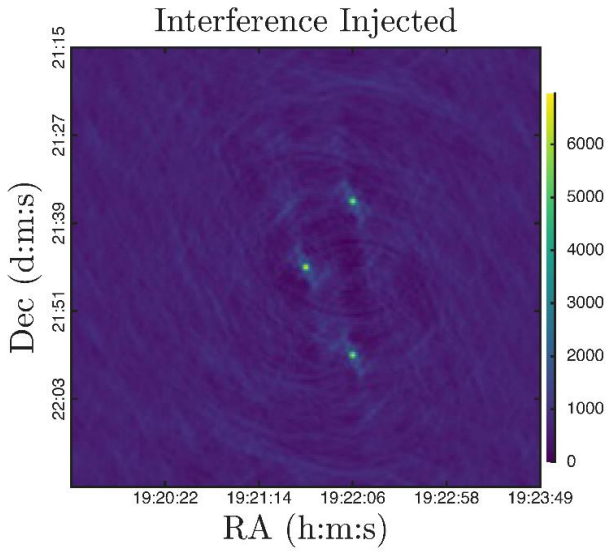
Output signals produced by the 3 RXs

- Alternatively, we can reconstruct the HDR signal via sparsity recovery, which offers better robustness against noise than high-order differences

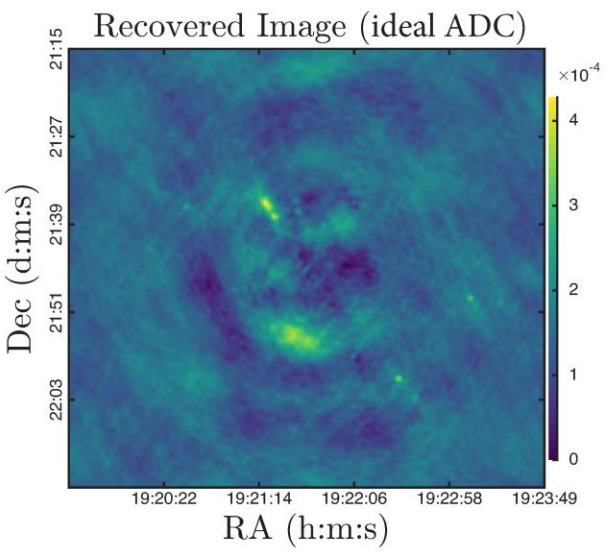
VLA Images with Satellite RFI



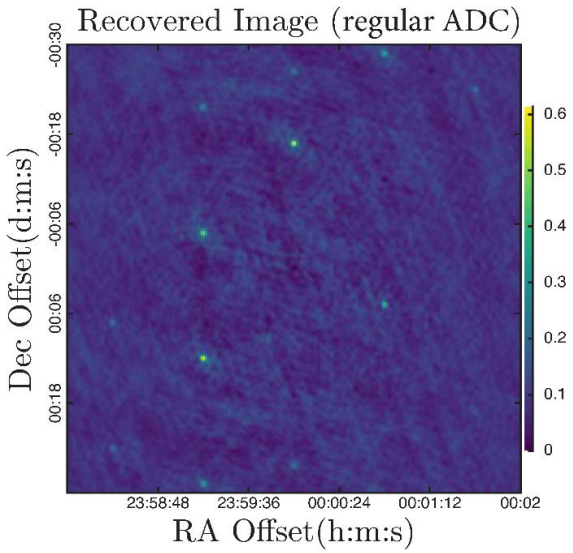
reference image



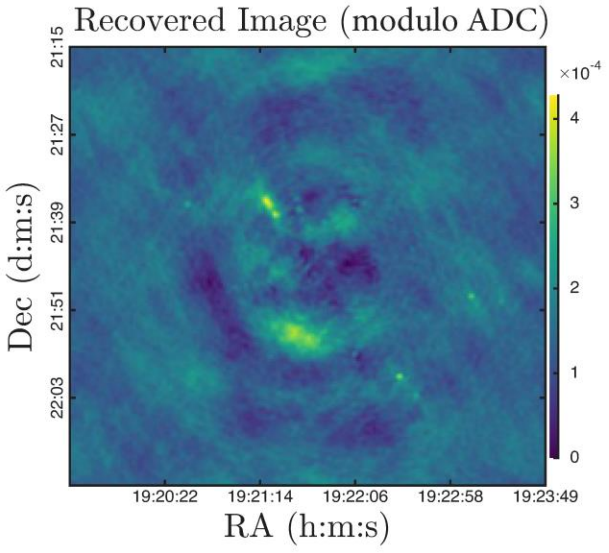
RFI injected



recovered image (ideal HDR ADC)

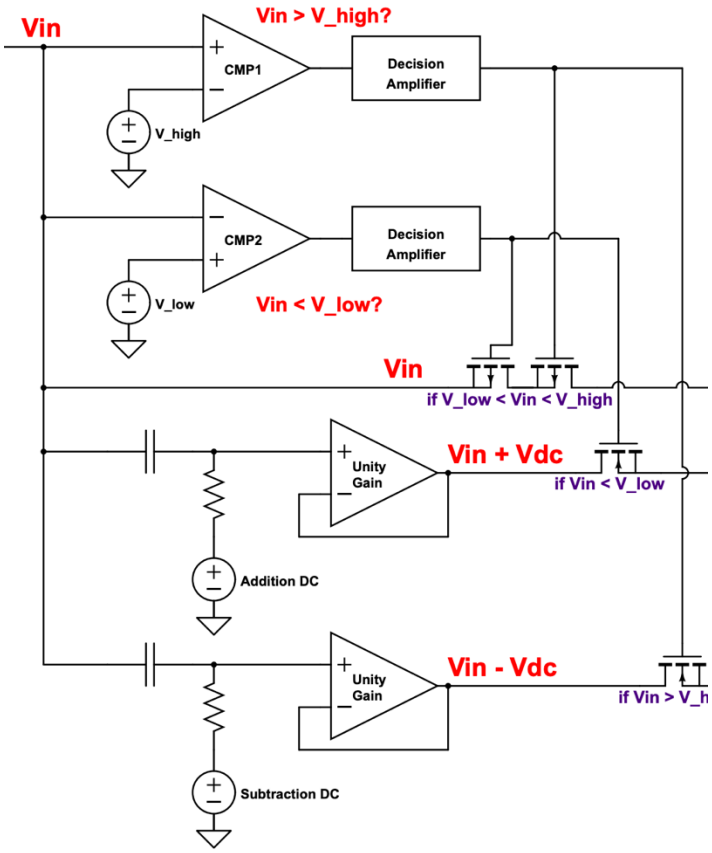


recovered image (regular LDR ADC)



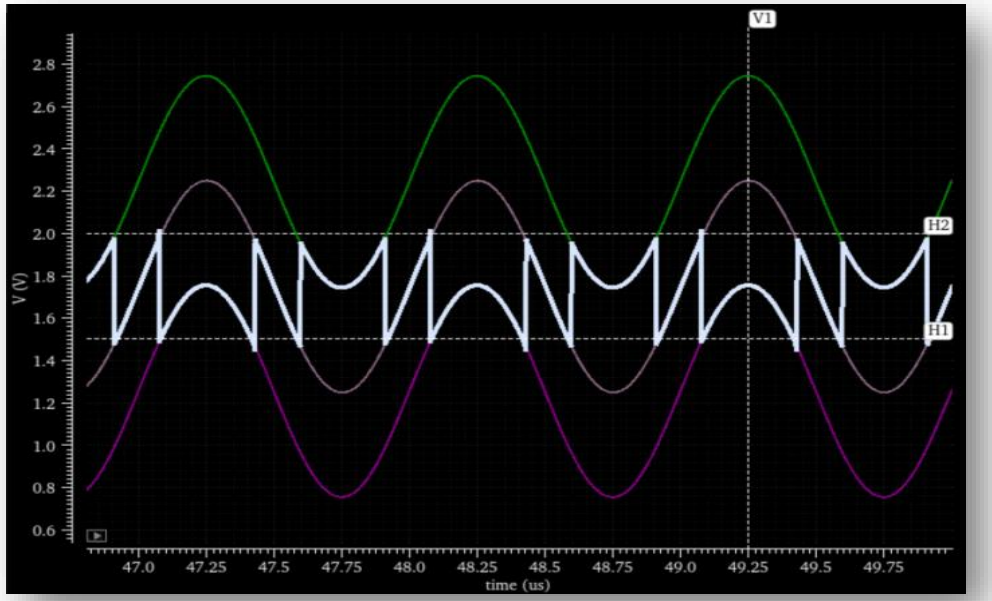
recovered image (modulo LDR ADC)

CMOS Folding Amplifier Progress



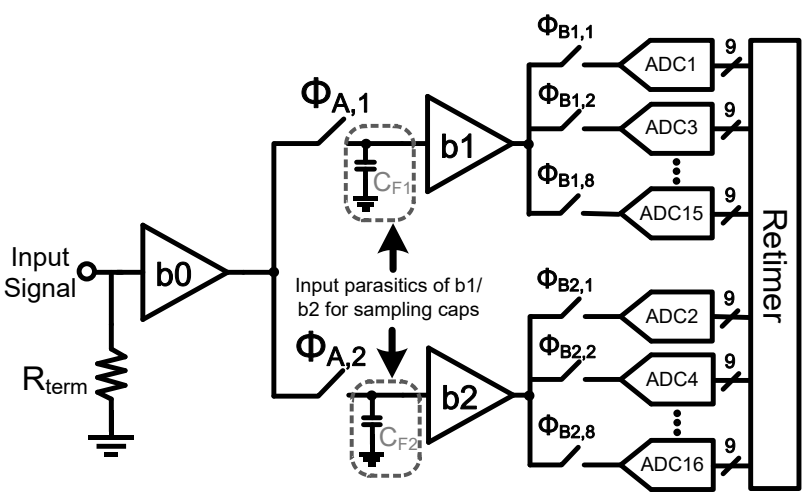
- Circuit achieves folding by running three concurrent signal lines at different DC levels and swapping between them depending on comparator output between the thresholds.

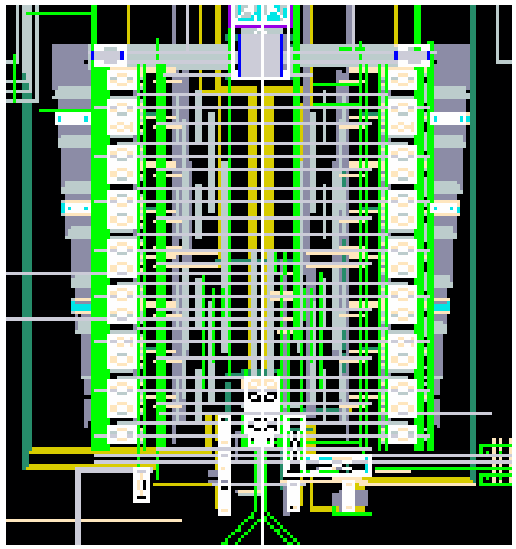
Simulation Results in Cadence

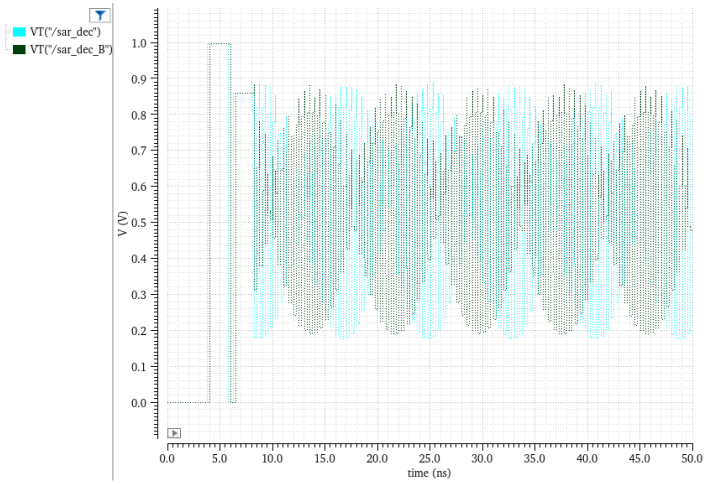


- Successfully simulated a high-speed sine wave at amplitude 0.5V and 1.75V DC, folding at 0.5Vpp with TSMC 65nm component models.**V**

CMOS ADC Progress







- Low supply voltage 8-bit ADC in CMOS process suitable for demonstrating signal distortion caused by interference.
- Physically implemented high-speed ADC for fabrication.
- Simulated ADC based on physical implementation (layout level).